Design of Segmented Digital to Analog Converter

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Abstract

In electronics, a **digital-to-analog converter** (**DAC** or **D-to-A**) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse operation. Signals are easily stored and transmitted in digital form, but a DAC is needed for the signal to be recognized by human senses or other non-digital systems.

A common use of digital-to-analog converters is generation of audio signals from digital information in music players. Digital video signals are converted to analog in televisions and mobile phones to display colors and shades. Digital-to-analog conversion can degrade a signal, so conversion details are normally chosen so that the errors are negligible.

Due to cost and the need for matched components, DAC are almost exclusively manufactured on integrated circuits (ICs). There are many DAC architectures which have different advantages and disadvantages. The suitability of a particular DAC for an application is determined by a variety of measurements including speed and resolution.

Introduction

Among the different implementations (R-2R ladder, switched capacitors, weighted current sources), a conversion structure based on the weighted type has been chosen. The main advantages associated with this current-steering architecture are:

-Easy integration in CMOS process.

-High speed.

-High energetic efficiency.

-Low silicon area.

And from the different methods to implement a weighted DAC (binary weighted, segmented), we have chosen an improved binary weighted current source solution which represents the best trade-off between speed, linearity and consumption.

Motivation and Goal

After doing my dissertation in M. tech VLSI on the topic of Digital to Analog converter I came to know there are lots of chances of research in DAC. Especially Segmented and current steering have more chances of more improvements are possible.

After doing M. Tech at nirma university IIT Bombay is best option to choose for PhD. Which help me to improve my knowledge and give me best and standard knowledge. In academic field knowledge and degree up gradation is more important. IIT Bombay have most valuable and knowledgeable faculty in VLSI design so I choose this university for further study here. I also believe that part time degree will not help me to get my best knowledge from IIT so I choose to apply for full time with my best effort I will get chance to prove myself.

Different Issues in Design

High speed.
Low power
Mismatch in DAC
Higher efficiency.
Easy integration in CMOS process
Low silicon area. Etc.

Statement of Purpose and Work Plan:

I have started to do some work on Different Architectures of DAC and till today most of works are on main architecture using Binary code and thermometer code only now my aim to Design DAC using 1's Complements, 2's Complements And more work on segmented DAC for to add different architectures. Till today most of work done on DAC using binary code as well as thermometer code which are easily implemented using R-2R architectures.

Proposed Design with Specifications:
My proposed design is to design DAC using current steering and R-2R DAC in one architecture and create segmented DAC .by doing it I want to improve following specifications Linearity, Resolution, INL, DNL, Offset and High Etc. next target is to develop new architecture using complements method and to add them in the Segmented DAC.

Summary:

New possibilities of the DAC Segmented Architecture using Thermometer, Current Steering and R-2R ladder Based DAC High Resolution and High Speed techniques can be designed for the future especially at lower Technology to go for new world of DAC. With the update of latest architecture which are designed by complements methods.

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